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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,630	10/12/2001	Taylor R. Efland	TI-31678	8387

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,630	EFLAND, TAYLOR R.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,10-16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-7, 10-16, 18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/19/2004 has been entered.

Election/Restrictions

2. Applicant's election without traverse of Group I in Paper No. 3 is acknowledged.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki et al. (US 5,973,554).

5. Regarding claim 1, Yamasaki (figs. 1-5) discloses a chip 71 having a first and second major opposing surfaces, a circuit having active components such as MOS transistor 70, and a protective overcoat 6 over the first chip surface. Yamasaki, also, shows a network of substantially coplanar power distribution lines 25 laterally disposed on the first surface of the chip over the overcoat and located directly over active

components of the circuit. The lines are conductively connected to the selected active components below the line in a direction normal to the first surface through vias 10 in the overcoat. Moreover, conductors 2b are connected to segments 2c of the lead frame (see fig. 1). As shown in figure 1, conductive members 66 directly connect the power distribution lines to connection regions external to the chip.

FIG. 1

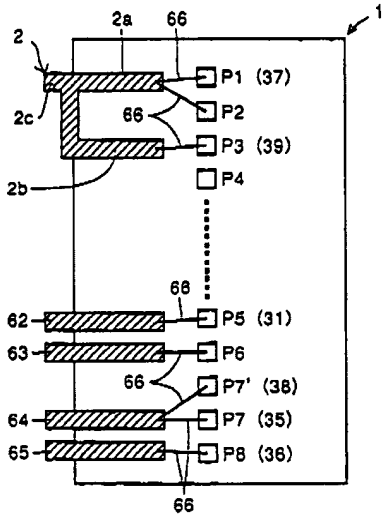
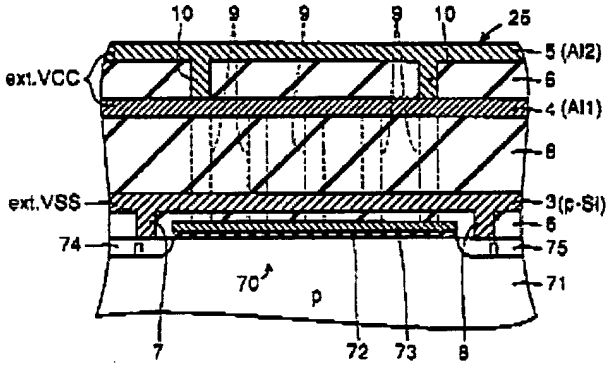


FIG. 2B



Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 3-5, 10, 12-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993).

8. Regarding claim 2, Yamasaki (*e.g.*, fig. 1 and 2) discloses a semiconductor device comprising;

- A semiconductor chip 71 having a first and second opposing surface, an active component 70 (MOS transistor);
- A metal layer 3 protected by a mechanically strong, electrically insulating overcoat 6 having a plurality of metal filled vias 9 to make an electrical contact;
- A plurality of windows to expose the circuit contact pads P1-P8 (*e.g.*, fig. 1);
- Electrically conductive substantially coplanar films (4, 5) laterally disposed deposited on the overcoat and patterned into a network of lines substantially vertically over the active components, the film is in contact with the vias 9 and having at least one stress absorbing film 4 and an outermost film 5 being non corrodible and metallurgical attachable.
- A lead frame (61-65) having a first plurality of segments providing electrical signal and a second plurality of providing power and ground;
- Electrical conductors 66 connecting the chip contact pads connecting the network lines and the plurality of segments.

The network pattern distributes the power current and the ground potential (*e.g.*, fig. 5). Yamasaki discloses that the chip is mounted in the lead frame. Nonetheless, Yamasaki fails to further specify that the semiconductor chip can be mounted in a chip mounting pad. Tani discloses a lead frame having inter alia a chip mounting pad. According to Tani this type of lead frame permits reliable bonding of semiconductor

chip, which prevents accidents due to the squeezing out of the preform material used, and which prevents wire distortion and shift of the leads or die pad during molding (col. 2/lls. 28-32). As shown in fig. 1 the second surface of the chip 3 is attached to the chip mounting pad 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the second surface of the semiconductor chip disclosed by Yamasaki to a lead frame having a chip mounting pad in accordance with Tani's invention in order to permit a reliable bonding of semiconductor chip and to avoid accidents due to the squeezing out of the preform material used, and to prevent wire distortion and shift of the leads or die pad during molding as taught by Tani.

9. Regarding claim 3, Yamasaki discloses that the chip is made of silicon (col. 2/lls. 64-66).

10. Regarding claim 5, Yamasaki discloses that the circuit comprises multi-layer metallization made of aluminum (col. 8/lls. 9-51).

11. Regarding claim 10, Tani discloses that the leads have a shape capable of being solderable to the outside parts or to the next packaging level substrate (*e.g.,* fig. 3).

12. Regarding claim 12, Yamasaki shows that the conductors/metallurgical attachments are bonding wires.

13. Regarding claim 13, Yamasaki shows that the stress absorbing metal layer 4 is made of aluminum (col. 8/lls. 9-51).

14. Regarding claim 14, Yamasaki shows that the outermost metal layer 5 is made of aluminum (col. 8/lls. 9-51).

15. Regarding claim 15, Yamasaki shows that the conductors 66 are bonding wires (*e.g.,* fig. 1).

16. Regarding claim 16, Tani discloses that the semiconductor chip is bonded to the leads radially disposed around the die pad with gold wires (col. 1/lls.19-28).

17. Regarding claim 18, Yamasaki shows that the network of lines is electrically connected to the segments that are suitable for outside electrical contact.

18. Regarding claim 19, Yamasaki shows that the network of lines, together with the metal filled vias provides a power distribution function to the active components.

19. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Applicant's Admitted Prior Art.

20. Regarding claim 7, Yamasaki in view of Tani shows most aspects of the instant invention. Yamasaki in view of Tani does not disclose that the lead frame is made from a material selected from a group consisting of copper, copper alloy, aluminum, iron nickel alloy or invar. However, Applicant's Admitted Prior Art discloses that it has been common practice to manufacture single piece lead frames from thin sheets of metal. For reasons of easy manufacturing, the commonly selected starting metals are copper, copper alloy, iron nickel alloys and invar (pp. 005). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the lead frame of Yamasaki in view of Tani of copper, copper alloy, iron nickel alloys or invar for easy manufacturing reasons as taught by Applicant's Admitted Prior Art.

21. Claims 6, 11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Wolf et al.

22. Regarding claim 6, Yamasaki discloses an overcoat layer 6 that function as interdielectric material. Yamasaki in view of Tani does not shows that the overcoat is made of one of silicon nitride, silicon oxynitride, silicon carbon alloys or polyimide. Wolf teaches that integrated circuits include a plurality of devices interconnected by multilevel interconnections separated by dielectric layers (pg 716-727). Also, the interconnect delay can be reduced by using low k dielectric material (*e.g.,* polyimide "second generation") having a dielectric constant of less than 2.5 (pgs. 791-795). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include multilevel interconnections having dielectric layers in the invention disclosed by Yamasaki in view of Tani to use a low k dielectric material such as polyimide which has a dielectric constant of less than 2.5 in order to reduce the interconnect delay as taught by Wolf.

23. Regarding claim 11, Yamasaki in view of Tani shows most aspects of the instant invention including lines and contacts pads attached to the outside part by conductors 66. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, Wolf teaches that the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the

same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

24. Regarding claim 15, Yamasaki in view of Tani shows most aspects of the instant invention including bonding wires conductors. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, Wolf teaches that the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

Response to Arguments

25. Applicant's arguments filed 07/27/2004 have been fully considered but they are not persuasive.

26. Applicant argues that that amended claims 1 and 2 are not taught by the prior art. Nonetheless, Yamasaki shows all the claimed limitations such as a network of substantially coplanar power distribution lines 25 disposed on the first surface of the chip over the overcoat 6 (see fig. 2B). Also, Yamasaki shows vias (*e.g.,* 10) connecting the lines and the active components, and electrically conductive members such as directly connecting the power distribution lines to connection regions external the chip (*e.g.,* 2a). Applicant argues that structure disclosed by Yamasaki is a single transistor structure. Nevertheless, Yamasaki teaches more than one transistor as clearly shown in figure 2b. Note that a sectional view means that the represented unit is repeated. This type of representation is used to avoid redundancy. Moreover, the top view evidenced that more than one transistor are used since several pairs of source/drain electrodes are depicted in figure 2A.

27. Applicant argues that Yamasaki in view of Tani does not teach a substantially, coplanar, laterally disposed films deposited on the overcoat and patterned into a network of lines substantially vertically over the active component. It is respectfully noted that these limitations are taught by Yamasaki in view of Tani (see paragraph 8)

28. Furthermore, applicant broadly argues that the limitations recited in claims 2, 3-5, 10, 12 –16, 18 and 19 are not taught by the prior art made of record. Nonetheless, each and every limitation recited in claims 3, 5,10, 12 –16, 18 and 19 are clearly shown by the prior art made of record (see paragraphs 10-21, 24 and 25). For example, Yamasaki discloses that the chip is made of silicon whereas the multi-layer metallization is made of aluminum (col. 2/lls. 64-66 & col. 8/lls. 9-51). If a prima facie case of

obviousness is established, the burden shifts to the applicant to come forward with arguments and/or evidence to rebut the prima facie case. See, e.g., Dillon, *919 F.2d at 692, 16 USPQ2d at 1901.* Rebuttal evidence and arguments can be presented in the specification, *In re Soni, 54 F.3d 746, 750, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995), by counsel, In re Chu, 66 F.3d 292, 299, 36 USPQ2d 1089, 1094-95 (Fed. Cir. 1995*), or by way of an affidavit or declaration under 37 CFR 1.132, e.g., Soni, 54 F.3d at 750, 34 USPQ2d at 1687; In re Piasecki, 745 F.2d 1468, 1474, 223 USPQ 785, 789-90 (Fed. Cir. 1984). However, arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., *In re Huang, 100 F.3d 135,139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).*

29. Applicant arguments regarding claim 7 have been considered. However, Yamasaki in view of Tani further in view of Applicant admitted prior art shows this limitation (see comments above)

30. Applicant broadly argues that the limitations recited in claims 6, 11 and 15 are not taught by the prior art. Nevertheless, Yamasaki in view of Tani further in view of Wolf teaches this limitations (see comments above)

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner

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SUPERVISORY PATENT EXAMINER
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Art Unit 2826

10/10/2004